2. The method of claim 1 wherein the creating the parameter functions comprises:

(a1) configuring each circuit of the plurality of circuits; and

(a2) generating values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions.

3. (AMENDED) The method of claim 2 wherein the constraint set includes constraint parameters having values selectable to meet the design constraints and the optimizing set includes optimizing parameters having values to be optimized.

4. (AMENDED) The method of claim 3 wherein selecting the new design points comprises:

(c1) selecting values of the constraint parameters to meet the design constraints;

(c2) determining values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

(c3) iterating c(1) and (c2) until values of the optimizing parameters are within a predetermined optimal range.

5. The method of claim 3 wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter.

6. The method of claim 5 wherein the design constraints include a delay constraint.

7. The method of claim 6 wherein (a1) comprises:

sizing components in each circuit.

8. The method of claim 6 wherein (a1) comprises:

selecting a design technology for each circuit, the design technology being one of static and dynamic technologies.

9. The method of claim 7 wherein (a2) comprises:

(a21) generating a circuit netlist representing the configured circuit;

(a22) generating a timing file based on the circuit netlist using a circuit critical path;

(a23) determining power of the configured circuit based on the circuit netlist;

(a24) calculating timing values by using a timing simulator; and

(a25) calculating power values by using a power estimator.

10. The method of claim 9 wherein selecting the new design points comprises:

(c1) selecting values of the delay parameter within the delay constraint;

(c2) determining values of the power parameter corresponding to the selected values of the delay parameter based on the parameter function; and

(c3) iterating (c1) and (c2) until values of the power parameter are within a predetermined optimal range.

11. (TWICE AMENDED) A machine readable medium having embodied thereon a computer program for processing by a machine, the computer program comprising:

(a) a first code segment to create parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, the parameter functions representing a relationship among design parameters of the subsystem, the design parameters including constraint and optimizing sets;

(b) a second code segment to select initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and

(c) a third code segment to select new design points on the parameter functions such that the second sum is improved within the design constraints.

12. (AMENDED) The machine readable medium of claim 11 wherein the first code segment comprises:

(a1) a code segment to configure each circuit of the plurality of circuits; and

(a2) a code segment to generate values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions.

13. (AMENDED) The machine readable medium of claim 12 wherein the constraint set includes constraint parameters having values selectable to meet the design constraints and the optimizing set includes optimizing parameters having values to be optimized.

14. (AMENDED) The machine readable medium of claim 13 wherein the third code segment comprises:

(c1) a code segment to select values of the constraint parameters to meet the design constraints;

(c2) a code segment to determine values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

(c3) a code segment to iterate (c1) and (c2) until values of the optimizing parameters are within a predetermined optimal range.

15. The machine readable medium of claim 13 wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter.

16. The machine readable medium of claim 15 wherein the design constraints include a delay constraint.

17. (AMENDED) The machine readable medium of claim 16 wherein (a1) comprises:

a code segment to size components in each circuit.

18. (AMENDED) The machine readable medium of claim 16 wherein (a1) comprises:

a code segment to select a design technology for each circuit, the design technology being one of static and dynamic technologies.

19. (AMENDED) The machine readable medium of claim 18 wherein (a2) comprises:

(a21) a code segment to generate a circuit netlist representing the configured circuit;

(a22) a code segment to generate a timing file based on the circuit netlist using a circuit critical path;

(a23) a code segment to determine power vectors of the configured circuit based on the circuit netlist;

(a24) a code segment to calculate timing values; and

(a25) a code segment to calculate power values.

20. (AMENDED) The machine readable medium of claim 19 wherein the third code segment comprises:

(c1) a code segment to select values of the delay parameter within the delay constraints;

(c2) a code segment to determine values of the power parameter corresponding to the selected values of the delay parameter based on the parameter function; and

(c3) a code segment to iterate (c1) and (c2) until values of the power parameter are within a predetermined optimal range.

21. (CANCELLED)

22. (THREE TIMES AMENDED) A system comprising:

a memory for storing program instructions;

a processor coupled to the memory to execute the program instructions, the program instructions when executed by the processor interacting with tools provided by a design environment causing the processor to at least

(a) create parameter functions for a plurality of circuits in a subsystem, the subsystem having design constraints, each one of the parameter functions corresponding to each one of the circuits, the parameter functions representing a relationship among design parameters of the subsystem, the design parameters including constraint and optimizing sets,

(b) select initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and

(c) select new design points on the parameter functions such that the second sum is improved within the design constraints.

23. (AMENDED) The system of claim 22 wherein the program instructions causing the processor to create the parameter functions causes the processor to:

(a1) configure each circuit of the plurality of circuits; and

(a2) generate values of design parameters for each circuit according to the configured circuit, the values providing the parameter functions.

24. (AMENDED) The system of claim 22 wherein the constraint set includes constraint parameters having values selectable to meet the design constraints and the optimizing set includes optimizing parameters having values to be optimized.

25. (AMENDED) The system of claim 24 wherein the program instructions causing the processor to select the new design points causes the processor to:

(c1) select values of the constraint parameters to meet the design constraints;

(c2) determine values of the optimizing parameters corresponding to the selected values of the constraint parameters based on the parameter functions; and

(c3) iterate (c1) and (c2) until values of the optimizing parameters are within a predetermined optimal range.

26. The system of claim 24 wherein the constraint parameters include a delay parameter and the optimizing parameters include a power parameter.

27. The system of claim 26 wherein the design constraints include a delay constraint.

28. A method comprising:

(a) generating first and second parameter functions for a circuit corresponding to first and second technologies, each of the first and second parameter functions relating a constraint parameter and an optimizing parameter;

(b) selecting a first initial design point and a first new design point on the first parameter function such that the first new design point corresponds to a first improved optimizing parameter within a design constraint;

(c) selecting a second initial design point and a second new design point on the second parameter function such that the second new design point corresponds to a second improved optimizing parameter within the design constraint; and

(d) selecting the first technology if the first improved optimizing parameter is better than the second improved optimizing parameter, else selecting the second technology.

29. The method of claim 28 wherein the first technology is a dynamic technology and the second technology is a static technology.